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10/689,716	10/22/2003	Nelson Gonzalez	19463-0002	3956

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HOGAN & HARTSON LLP
IP GROUP, COLUMBIA SQUARE
555 THIRTEENTH STREET, N.W.
WASHINGTON, DC 20004

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
03/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

dcptopatent@hhlaw.com
rogruwell@hhlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/689,716	GONZALEZ ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,29,30,32-34,41,44-48 and 50-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,29,30,32-34,41,44-48 and 50-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on March 9, 2009 has been entered.

Response to Arguments

2. Applicant's arguments filed March 9, 2009 are fully considered but are not persuasive.

3. As per Claim 1, Applicant argues Levy (US 20040088469A1) fails to suggest plurality of high speed video card slots including first and second high-speed video card slot interconnected to motherboard via scalable interconnect and switch system that operate to form distributed links of lanes during operation. Levy does not provide any disclosure regarding attachment and operation of two or more high speed video cards (p. 11).

In reply, Examiner points out according to Applicant's disclosure, "high speed video card slot" is defined as PCI Express video card slot [00057]. Levy teaches one or more devices (DEVICES 1-5) comprise video cards [0016]. Device interfaces of DEVICES 0-5 comprise ports that provide physical interface for establishing lanes between devices. Link comprises lanes which are grouped together to form communications path between devices [0018]. These links are PCI Express links [0001]. So, Levy teaches video cards are connected to system through PCI

Express links, and so Levy is considered to teach PCI Express video card slots, which are high speed video card slots. Even though Levy does not explicitly teach more than one video card is attached to their respective video card slots at a time and video cards operate in parallel, Grimaud (US005546530A) was used to teach attaching first and second video card to at least one first video card slot and second video card slot, respectively, wherein first and second video cards operate in parallel to output graphics data to single visual display device (*card slots so that users may add processors as desired*, c. 2, ll. 40-44, *after the plurality of processors compute their respective images, the image data is communicated to a buffer, buffer combines the image data into a single image frame which is then stored in a frame buffer*, c. 2, ll. 53-65; *processors operate simultaneously on different portions of the image*, c. 7, ll. 39-40). Therefore, the device of Levy can be modified so that more than one video card is attached to their respective high speed video card slots at a time and than the video cards operate in parallel, as suggested by Grimaud. Therefore, the combination of Levy and Grimaud is considered to teach a plurality of high speed video card slots as recited in Claim 1. Levy does teach a switch system that operates to form distributed links of lanes during operation, as discussed directly below.

4. Applicant argues switch 116 of Levy does not allocate bandwidth but only assists with turning device on or off. Levy does not teach switch forms distributed links which contain lanes distributed by switch during operation in response to bandwidth needs of video cards during processing (p. 12).

In reply, Examiner points out that Levy describes performing port identification to define lanes of links between devices, and assigns certain number of lanes to each link. Port identification methods provide system designer with fine grain control of bandwidth between

devices by allowing system designer to assign lanes to links on per lane basis [0075]. One or more devices (DEVICES 1-5) comprise video cards [0016]. Levy describes devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, a root reset or a request to re-identify its ports. The device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but during operation (the devices may initiate their port identification methods in response to other events such as, for example, a root reset or a request to re-identify its ports [0042]). So, Levy teaches switch forms distributed links which contain lanes distributed by switch during operation in response to bandwidth needs of video cards during processing [0075, 0016, 0042].

5. As per Claim 3, Applicant argues that Levy does not provide a switch that dynamically distributes (as opposed to merely splits) the bandwidth (p. 13).

In reply, the Examiner points out that Levy describes devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, a root reset or a request to re-identify its ports. The device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but can be redistributed several times during operation, whenever there is a root reset or a request to re-identify its ports [0042]. Therefore, the lanes are dynamically distributed. Therefore, Levy teaches a switch that dynamically distributes the bandwidth [0075, 0042].

6. As per Claim 7, Applicant argues Levy does not teach using switch to distribute 24 lanes from interconnect dynamically during operation of motherboard into one x8 and one x16 connection (p. 14).

In reply, the Examiner points out that Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect having a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation [0075, 0042] into x8 connection between chipset (104, Fig. 1) and one of plurality of high-speed video card slots and x16 connection between chipset and another of plurality of high-speed video card slots [0001, 0016].

7. As per Claim 29, Applicant argues that Levy does not teach a second smaller-scaled connection to the second video card slot (p. 14).

In reply, the Examiner points out that Levy teaches interconnect supports links between chips that have x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches wherein the switch allocates 1st x16 connection to 1st video card slot and 2nd smaller-scaled connection to 2nd video card slot [0075, 0001, 0016].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 3-7, 29, 30, 32-34, 41, 44-48, and 50-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1), Stufflebeam (US006295566B1), and Grimaud (US005546530A).

11. As per Claim 1, Levy teaches chipset (104) for managing data transfers within computing device [0014]; scalable interconnect (Device 0) connecting to computing device [0021], scalable interconnect supporting a number of interconnect lanes [0021, 0018]; plurality of ports or high-speed video card slots [0016] connected to interconnect [0021], high speed video card slots including at least one 1st video card slot and 2nd video card slot [0016]. According to Applicant's disclosure, "high speed video card slot" is defined as PCI Express video card slot [00057]. Levy teaches one or more devices (DEVICES 1-5) comprise video cards [0016]. Device interfaces of DEVICES 0-5 have ports that provide physical interface for establishing lanes between devices. Link comprises lanes which are grouped together to form communications path between devices [0018]. These links are PCI Express links [0001]. So, Levy teaches video cards are connected to system through PCI Express links, and so Levy is considered to teach PCI Express video card slots, which are high speed video card slots. Levy teaches switch (116) connected to interconnect and adapted to convert interconnect lanes into plurality of distributed links such that there is a

different one of distributed links providing connection to each of plurality of high-speed video card slots [0021, 0017, 0018, 0016]. Levy teaches performing port identification to define lanes of links between devices, and assigns certain number of lanes to each link. Port identification methods provide system designer with fine grain control of bandwidth between devices by allowing system designer to assign lanes to links on per lane basis [0075]. One or more devices (DEVICES 1-5) comprise video cards [0016]. Devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, root reset or request to re-identify its ports. Device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but during operation (devices may initiate their port identification methods in response to other events such as, for example, root reset or request to re-identify its ports [0042]). So, Levy teaches switch is configured to distribute lanes dynamically during operation to plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by video cards [0075, 0016, 0042].

However, Levy does not teach computing device is motherboard and motherboard enables first and second card to attach, respectively, to at least one first card slot and second card slot, and motherboard enables first and second card to operate concurrently to output data. However, Stufflebeam teaches interconnect connecting to motherboard (*host bus 110 typically is located on a motherboard*, c. 4, ll. 48-50; *memory controller 200 provides interconnection between the host bus 110*, c. 4, ll. 59-61); and plurality of high-speed card slots connected to interconnect (c. 6, ll. 23-35). When user wishes to attach additional card, power is removed from card slot that card is to be attached to. After inserting card into slot, the software identifies and

configures the additional card in the slot so that the first and second card can operate in parallel to output data (*power-down applet receives signal from a user indicating a user desire to insert an additional card into a PCI slot*, c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; *processing parallelism*, c. 1, ll. 21-25), and the cards can include video cards (c. 5, ll. 7-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Levy so computing device is motherboard as suggested by Stufflebeam. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new features to machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. Motherboard, by enabling pluggable components, allows users to personalize a computer system depending on their applications and needs. It would have been obvious to modify Levy so motherboard enables 1st and 2nd card to attach, respectively, to at least one first card slot and second card slot, and motherboard enables first and second card to operate concurrently to output data because Stufflebeam suggests faster processing (c. 1, ll. 21-25).

However, Levy and Stufflebeam do not expressly teach both cards are video cards, and video cards output graphics data to a single visual display device. However, Grimaud teaches attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (c. 2, ll. 40-44, c. 2, ll. 53-65; c. 7, ll. 39-40).

It would have been obvious to modify devices of Levy and Stufflebeam so display area of display is divided into first and second sections, first video card performing graphics processing related to first section; and second video card performing graphics processing related to second section as suggested by Grimaud because Grimaud suggests this ensures single graphics element

is not overburdened with its rendering task by allowing dynamic adjustment of each graphics element so graphics elements take approximately the same time to render their respective images, and video cards can operate on these divided sections in parallel, therefore allowing different graphics machines to be connected together to render complex images faster than any one of them taken separately would be able to render (c. 5, ll. 55-c. 6, ll. 12; c. 7, ll. 10-40).

12. As per Claims 3, 53, and 55, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection and said first and second high-speed video card slots are each physically configured as x16 video card slots, and wherein the switch (116, Fig. 3) dynamically distributes bandwidth from the x16 connection to two x16 video card slots via said distributed links [0001, 0021, 0017, 0018, 0016, 0075, 0042]. Levy describes devices may initiate their port identification methods in response to events other than in response to power on reset, such as, for example, a root reset or a request to re-identify its ports. The device ID of the device may be set by reset hardware of the device, or may be set by some other mechanisms [0042]. So, lanes are distributed not only during startup or other one-time configuration of machine, but can be redistributed several times during operation, whenever there is a root reset or a request to re-identify its ports [0042]. So, the lanes are dynamically distributed. So, Levy teaches a switch that dynamically distributes the bandwidth [0075, 0042].

13. As per Claim 4, Levy teaches interconnect comprises at least a x32 connection [0001].

14. As per Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1

links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Fig. 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

15. As per Claim 6, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001, 0016].

16. As per Claims 7, 54, and 56, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches interconnect having a connection having at least 24 lanes, and wherein said switch dynamically distributes lanes at any given time during operation [0075, 0042] into x8 connection between chipset (104, Fig. 1) and one of plurality of high-speed video card slots and x16 connection between chipset and another of plurality of high-speed video card slots [0001, 0016].

17. As per Claim 29, Levy teaches interconnect supports links between chips that have x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches wherein the switch allocates 1st x16 connection to 1st video card slot and 2nd smaller-scaled connection to 2nd video card slot [0075, 0001, 0016].

18. As per Claims 30 and 46, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at

least x1 links, leaving chips to optionally support the other link widths. Levy gives an example wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

19. As per Claims 32 and 47, Levy teaches that the interconnect (Device 0) connects to Devices 1-5. Devices 1-5 could be Ethernet cards, video cards, RAID controllers, SCSI controllers, ATA disk controllers, PCI bridges, etc. [0016]. Therefore, it would be obvious to one of ordinary skill in the art that Device 1 and Device 2 could each be a video card, and Device 3 could be a peripheral. Levy describes that the device interfaces of the Devices 0-5 support lane reordering. For example, the device interface of Device 0 may support up to 4 links, and Device 1 may support up to 3 links [0020]. For example, Link 1 consists of three lanes, Link 2 consists of two lanes, Link 3 consists of two lanes, Link 4 consists of one lane, and Link 5 consists of one lane [0075]. Since the device interfaces of the Devices 0-5 support lane reordering [0020], it would be obvious to one of ordinary skill in the art that the dimensions of the lanes can be specified to be any dimension that is needed to support cards and peripherals of various dimensions. Therefore, Device 1 and Device 2 could have first prespecified dimensions, and Device 3 could have second prespecified dimensions. Therefore, it would be obvious to one of ordinary skill in the art from the device of Levy to further comprise a peripheral slot connected to the interconnect (Device 0), wherein the first video card slot and the second video card slot have first prespecified dimensions and the peripheral slot has second prespecified dimensions, wherein the second dimensions differs from the first dimensions [0016, 0020, 0075].

However, Levy does not expressly teach that two cards are video cards. However, Grimaud teaches attaching a first and a second video card to at least one first video card slot and

second video card slot, respectively (c. 2, ll. 40-44, c. 2, ll. 53-65; c. 7, ll. 39-40). This would be obvious for the reasons given in the rejection for Claim 1.

20. As per Claim 33, Levy teaches that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy teaches wherein the first video card slot and the second video card slot have first prespecified dimensions [0016, 0020, 0075], as discussed in the rejection for Claim 32, and wherein the first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots [0016, 0020].

21. As per Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

22. A per Claim 41, Levy teaches computing device for supporting multiple video cards, computing device having processor socket 104 adapted to receive processor 102 [0014]; single scalable interconnect (Device 0) provides data paths to processor socket (Fig. 1), said scalable interconnect supporting a number of interconnect lanes [0021, 0018]; plurality of high-speed video card slots connected to interconnect, each video card slot has first prespecified dimensions and is specifically adapted for coupling to video card [0001, 0021, 0016]. Levy teaches a switch (116) connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots [0021, 0017, 0018, 0016], and wherein said switch is configured to distribute lanes dynamically during operation to said

plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards [0075, 0016, 0042].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data. However, Stufflebeam describes that the computing device is a motherboard (c. 4, ll. 48-50), the processor is a central processing unit (CPU) (100, Fig. 1; c. 4, ll. 40-46), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data (c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; c. 1, ll. 21-25), wherein the cards can include video cards (c. 5, ll. 7-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so the processor is a CPU as suggested by Stufflebeam. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. It would have been obvious to modify the device so that the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data for the same reasons given in the rejection for Claim 1.

However, Levy and Stufflebeam do not teach that the cards are substantially similar video cards and operate to output graphics data to a single visual display device. However, Grimaud teaches this limitation, as discussed in the rejection for Claim 1.

23. As per Claim 44, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links,

leaving chips to optionally support other link widths, so, Levy teaches each of video card slots is configured to couple with graphics card designed to be used with x16 connection [0001, 0016].

24. As per Claim 45, Levy teaches interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support other link widths. So, Levy teaches an interconnect (Device 0, Fig. 1) and said switch produce a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

25. As per Claim 48, Levy teaches high performance computer including scalable interconnect (Device 0) that supports number of interconnect lanes [0021, 0018], scalable interconnect connects to first and second high-speed video card slots via switch, first and second high-speed video card slots having substantially similar physical configuration [0001], as discussed for Claim 42, and video slot physical configuration is selected to allow first and second high-speed video card slots each to accept a graphics card; and first graphics card coupled to first high-speed video card slot [0016]; the following occurs during operation of said computer: said switch converts said interconnect lanes into two distributed links such that there is a different one of said distributed links connecting to each of said plurality of high-speed video card slots [0021, 0017, 0018, 0016], and switch distributes lanes to said distributed links in response to current bandwidth needs of said graphics cards during processing by said cards [0075, 0016, 0042].

However, Levy does not teach computing device is motherboard, processor is central processing unit (CPU), and second graphics card coupled to second high-speed video card slot, wherein the following occurs during operation of said computer: said first and second graphics

cards operate concurrently to output graphics data to a display device. However, Stufflebeam teaches that the computing device is a motherboard (c. 4, ll. 48-50), the processor is a CPU (100, Fig. 1; c. 4, ll. 40-46), and a second card coupled to the second slot, wherein the following occurs during operation so said computer: said first and second cards operate concurrently to output data (c. 3, ll. 31-33, c. 3, ll. 56-c. 4, ll. 17; c. 1, ll. 21-25), wherein the cards can include high-speed graphics cards (c. 5, ll. 7-19). This would be obvious for reasons for Claim 41.

26. As per Claims 50-52, Levy does not teach a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section. However, Grimaud teaches a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section (c. 2, ll. 40-44, 53-65). This would be obvious for the same reasons given in the rejection for Claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Joni Hsu/
Examiner, Art Unit 2628